WHAT IS CLAIMED IS:

1. A power management process, to control a power state of a computer system that comprises a CPU, a chipset, a system RAM and a BIOS ROM, wherein the BIOS ROM comprises a BIOS program to initialize the computer system, the power management process comprising:

detecting whether a power management event occurs;

generating a system interrupt when the power management event occurs;

providing a first memory address segment with a memory space to the system RAM to execute a service routine of the system interrupt of the BIOS program;

driving the CPU to execute the service routine of the system interrupt irrelevant to the system RAM at the first memory address segment of the system RAM via the BIOS program;

driving the CPU to execute a service program of the system interrupt to synchronize an operation frequency of the system RAM with an operation frequency of the CPU at a memory address segment of the BIOS ROM; and

executing a power management control command to drive the computer system to enter a specific sleeping state.

2. The power management process according to claim 1, wherein the computer system includes an advance configuration power interface (ACPI) computer system.

3 The power management process according to claim 1, wherein the chipset comprises a chip enable circuit controlled by the CPU to output a signal to enable the BIOS ROM.

4. The power management process according to claim 1, wherein generating the system interrupt includes outputting a system interrupt control signal from the chipset to the CPU.

5. The power management process according to claim 1, wherein before generating the system interrupt further comprises:

configuring the power management control command at a specific I/O address; and

configuring an I/O trap at the specific I/O address.

6. The power management process according to claim 1, wherein the chipset further comprises a decoder to decode a plurality of memory addresses of the system RAM and a shadow RAM control register to control a decode sequence of the decoder.

7. The power management process according to claim 6, wherein executing the service routine to synchronize the operation frequencies of the CPU and the system RAM includes using the BIOS program to program the shadow RAM control register, so as to enable the BIOS ROM.

8. The power management process according to claim 1, further comprising:

detecting whether a wake-up event occurs;

initializing and arranging the CPU, the chipset and the system RAM when the wake-up event occurs;

generating a system interrupt;

driving the CPU to resume a hardware state information of the computer system via the BIOS program; and

leaving the system interrupt.

9. The power management process according to claim 1, wherein the system interrupt includes a system control interrupt.

10. The power management process according to claim 2, wherein the specific sleeping state includes a S3 sleeping state.

11. A power management process, to control a power state of a computer system that comprises a CPU, a chipset, a system RAM and a BIOS ROM, wherein the BIOS ROM comprises a BIOS program to initialize the computer system, the power management process comprising:

detecting whether a power management event occurs;

using a software interrupt interface provided by the BIOS system program to generate a system interrupt when the power management event occurs;

providing a first memory address segment with a memory space to the system RAM to execute a service routine of the system interrupt of the BIOS program;

driving the CPU to execute the service routine of the system interrupt irrelevant to the system RAM at the first memory address segment of the system RAM via the BIOS program;

driving the CPU to execute a service program of the system interrupt to

synchronize an operation frequency of the system RAM with an operation frequency of the CPU at a memory address segment of the BIOS ROM; and

executing a power management control command to drive the computer system to enter a specific sleeping state.

12. The power management process according to claim 11, wherein the computer system includes an advance power management (APM) computer system.

13. The power management process according to claim 11, wherein the chipset comprises a chip enable circuit controlled by the CPU to output a signal to enable the BIOS ROM.

14. The power management process according to claim 11, wherein generating the system interrupt includes outputting a system interrupt control signal from the chipset to the CPU.

15. The power management process according to claim 11, wherein the chipset further comprises a decoder to decode a plurality of memory addresses of the system RAM and a shadow RAM control register to control a decode sequence of the decoder.

16. The power management process according to claim 15, wherein executing the service routine to synchronize the operation frequencies of the CPU and the system RAM includes using the BIOS program to program the shadow RAM control register, so as to enable the BIOS ROM.

17. The power management process according to claim 11, further comprising:

detecting whether a wake-up event occurs;

initializing and setting up the CPU, the chipset and the system RAM when the wake-up event occurs;

generating a system interrupt;

driving the CPU to resume a hardware state information of the computer system via the BIOS program; and

withdrawing from the system interrupt.

18. The power management process according to claim 11, wherein the system interrupt includes a system management interrupt.

19. The power management process according to claim 12, wherein the specific sleeping state includes a STR sleeping state.